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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,698	08/15/2000	Ki Jun Kim	HI-006	1780

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EXAMINER	
DADA, BEEMNET W	
ART UNIT	**PAPER NUMBER**
2135	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/637,698	KIM ET AL.	
	Examiner	Art Unit	
	Beemnet W. Dada	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-18 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14,15,17,18 and 20-25* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in reply to an amendment filed on April 04, 2006. Claims 1, 4, 7 and 14 have been amended, claim 19 has been cancelled and new claim 25 has been added. Claims 1-12, 14-18 and 20-25 are pending.

Response to Arguments

2. Applicant's arguments filed April 04, 2006 have been fully considered but they are not persuasive.

3. With respect to claims 1 and 14, Applicant argued that Dahlman et al fails to teach setting an initial value of a scrambling code generator to a binary value of n when a n-th one of the plurality of primary scrambling codes is to be generated from the scrambling code generator. Applicant further argues that Ogawa et al fails to teach shifting an nth primary code by m times to generate a secondary scrambling code. Examiner disagrees.

Examiner would point out that Dahlman et al teaches setting a starting values of a scrambling code generator for normal transmission and slightly modifying the starting values for a slotted transmissions and loading the slightly modified values as a starting values in the scrambling code generator, for generating a desired scrambling code [see column 4, lines 40 - column 5, lines 9]. Furthermore, Ogawa et al teaches a scrambling code generator for generating primary and secondary scrambling codes, wherein the secondary scrambling codes are generated by shifting the primary scrambling codes (see for example, col 7-8, "...the shift register SR2 which occurs in synchronism with the clock CLK from the clock generator 39, the exclusive OR XR23 generates **an M-series of a type which is different from the first M-series**...") [see Ogawa et al. column 7, lines 37-coumn 8, line 10].

4. With respect to claims 4 and 7, Applicant argues that the art on record fails to teach generating an initial value of a secondary scrambling cod by shifting an nth primary scrambling code and further argued that the art on record fails to teach "a masking function unit, which receives...an n-th primary scrambling code by m times." Examiner disagrees.

Examiner would point out that Dahlman teaches generating scrambling codes by performing binary addition of the output from the second shift register to an output from the first shift register (figure 4, and column 4, lines 58-67). Burns teaches a masking function unit, which receives respective outputs from shift registers, and performs a masking function for the received data to output data for the generation of scrambling code (column 8, lines 29-44). And as discussed above, Ogawa et al teaches a scrambling code generator for generating primary and secondary scrambling codes, wherein the secondary scrambling codes are generated by shifting the primary scrambling codes (see for example, col 7-8, "...the shift register SR2 which occurs in synchronism with the clock CLK from the clock generator 39, the exclusive OR XR23 generates **an M-series of a type which is different from the first M-series**...") [see Ogawa et al. column 7, lines 37-coumn 8, line 10].

Examiner would further point out that TSG-Ran teaches a masking function unit, which receives respective outputs from the first shift register, (figure 5, masking function units, and outputs from register 1 and register 2 to the masking function units), and performs a masking function for the received data to output data for the generation of the secondary scrambling code (figure 5, masking function unit), wherein the primary scrambling code is generated by performing a binary addition of the output from the second shift register to an output from the first shift register (figure 5, outputs from register 1 and register 2 combine in the circle plus and output primary scrambling code), and the secondary scrambling code is generated by performing a binary addition of the output from the masking function unit to the output from the

second shift register (figure 1, outputs from register 2 and masking unit combine in the circle plus and output secondary scrambling code). Tsg-Ran teaches an 18 bit shift registers having data outputs (figure 5, outputs from shift registers 1 and 2). Examiner asserts that the art on record teaches the claim limitations and therefore the rejection is respectfully maintained.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 14, 15, 20-21 and 24 are rejected under 35 U.S.C 103 (a) as being unpatentable over Dahlman et al. (hereinafter Dahlman) (U.S. Patent 6,339,646 B1) in view of Ogawa et al. US Patent 6,738,411 B1 (hereinafter Ogawa).

7. As per claims 1 and 14, Dahlman teaches a method of generating multiple scrambling codes in a communication system, in which each of a plurality of base stations use one of a plurality of primary scrambling codes and one of a plurality of secondary scrambling code sets, each secondary scrambling code set having a plurality of secondary scrambling codes, comprising:

setting (loading) an initial value of a scrambling code generator to a binary value of "n" when a n-th one of the plurality of primary scrambling codes is to be generated from the

scrambling code generator to generate a desired primary scrambling code (column 4, line 64 - column 5, line 9); and

setting (loading) an initial value of the scrambling code generator with a value obtained by shifting (clocking) to generate a secondary scrambling code. Dahlman teaches shifting the shift register to generate a secondary scrambling code (column 4, lines 64-67, column 5, lines 1-5). Dahlman further teaches a method of generating primary and secondary scrambling codes by shifting (clocking) shift registers (column 4, lines 64-67, column 5, lines 1-5). However, Dahlman does not clearly teach shifting the nth primary scrambling code by m times to generate a secondary scrambling code.

Ogawa teaches a method for simultaneous plural code series generator and for generating primary and secondary scrambling codes [see abstract] further including shifting the nth primary scrambling code by m times to generate an initial value of an m-th secondary scrambling code [column 7, line 37-column 8, line10 and figure 5]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings of Ogawa within the system of Dahlman in order to increase efficiency of the system.

8. As per claim 3, Dahlman teaches a method of generating multiple scrambling codes, comprising:

generating a plurality of primary scrambling codes (column 5, claim 1);

for each of the plurality of primary scrambling codes, generating primary and secondary scrambling codes by shifting (clocking) shift registers (column 4, lines 64-67, column 5, lines 1-5).

comparing each of the plurality of primary scrambling codes to an initial value of each of the secondary scrambling codes (column 4, lines 23-33 and figure 1); and

Furthermore, Dahlman teaches a method generating Gold codes, which ensure that the output sequences from shift registers are different from starting values (column 4, lines 40-45).

Dahlman further teaches a method of generating primary and secondary scrambling codes by shifting (clocking) shift registers (column 4, lines 64-67, column 5, lines 1-5). However, Dahlman does not clearly teach shifting the nth primary scrambling code by m times to generate a secondary scrambling code.

Ogawa teaches a method for simultaneous plural code series generator and for generating primary and secondary scrambling codes [see abstract] further including shifting the nth primary scrambling code by m times to generate a secondary scrambling code [column 7, line 37-column 10 and figure 5]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings of Ogawa within the system of Dahlman in order to increase efficiency of the system.

9. As per claims 2 and 15, Dahlman further teaches the method, wherein the initial value of the scrambling code generator is set by setting a 7-th and 11-th bits included in the initial value to a value of 1, setting a first through 10-th bits, except for the 7-th and 11-th bits, to an 8 bit binary expression of "n," and setting, remaining ones of the bits, other than the first through 11-th bits, to a value of "0" (column 5, lines 4-17 and figure 4).

10. As per claims 20, 21 and 24, Ogawa further teaches the method wherein the primary scrambling code and the secondary scrambling code are generated concurrently [column 7, line 37-column 10 and figure 5].

11. Claims 4-12, 22 and 23 are rejected under 35 U.S.C 103 (a) as being unpatentable over Dahlman (U.S. Patent 6,339,646 B1) in view of Burns (U.S. Patent No. 6,141,374) and further in view of Ogawa et al. US Patent 6,738,411 B1 (hereinafter Ogawa).

12. As per claims 4 and 7, Dahlman teaches a forward multiple scrambling code generating apparatus, comprising:

a first shift register (figure 4, unit 202), which shifts bits of a bit stream by one bit in response to every input of an external unit clock, respectively, and outputs data for the generation of a primary scrambling code (column 4, line 67, and column 5, lines 1-2);

a second shift register (figure 4, 204), which shifts bits of a bit stream by one bit in response to every input of an external unit clock, respectively, and outputs data for the generation of the primary scrambling code and a secondary scrambling code (column 4, line 67, and column 5, lines 1-2);

Furthermore, Dahlman teaches generating scrambling codes by performing binary addition of the output from the second shift register to an output from the first shift register (figure 4, and column 4, lines 58-67). Dahlman also teaches a method of utilizing gold codes to ensure output sequences generated from shift registers are different (column 4, lines 40-45). However Dahlman does not explicitly teach a masking function unit, which receives respective outputs from the first shift register, and performs a masking, function for the received data to output data for the generation of the secondary scrambling code.

Burns teaches a masking function unit, which receives respective outputs from shift registers, and performs a masking function for the received data to output data for the generation of scrambling code (column 8, lines 29-44). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement a masking function unit as taught by Burns into the scrambling code generator of Dahlman in order to generate secondary scrambling codes which are different from the primary scrambling codes.

Dahlman further teaches a method of generating primary and secondary scrambling codes by shifting (clocking) shift registers (column 4, lines 64-67, column 5, lines 1-5). However, the combination of Dahlman and Burns does not clearly teach shifting the nth primary scrambling code by m times to generate a secondary scrambling code.

Ogawa teaches a method for simultaneous plural code series generator and for generating primary and secondary scrambling codes [see abstract] further including shifting the nth primary scrambling code by m times to generate a secondary scrambling code [column 7, line 37-column 10 and figure 5]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings of Ogawa within the system of Dahlman-Burn in order increase efficiency of the system.

13. As per claims 5, 9 and 10, Dahlman further teaches the apparatus, wherein the first shift register comprises an 18 bit register (figure 4, unit 202), in which a value obtained after a binary addition of an output of a 0-th one of the 18 bits to an output of a 7-th one of the 18 bits is fed back to a 17-th one of the 18 bits (figure 4).

14. As per claims 6, 11, and 12, Dahlman further teaches the apparatus, wherein the second shift register comprises an 18 bit register (figure 4, unit 204), in which a value obtained after a

binary addition of outputs from a 0-th, 5-th, 7-th, and 10-th one of the 18 bits is fed back to a 17-th one of the 18 bits (figure 4).

15. As per claim 8, Burns further teaches the apparatus, wherein the register output and the second register output are combined using binary addition, and the second register output and the masking output are combined using binary addition (column 8, lines 34-44).

16. As per claims 22 and 23, Ogawa further teaches the method wherein the primary scrambling code and the secondary scrambling code are generated concurrently [column 7, line 37-column 10 and figure 5].

17. Claims 17, 18 and 25 are rejected under 35 U.S.C 103 (a) as being unpatentable over Dahlman et al. (hereinafter Dahlman) (U.S. Patent No. 6,339,646 B1) in view of Ogawa et al. US Patent 6,738,411 B1 (hereinafter Ogawa) and further in view of TSGR1#6(99)915, "TSG-RAN Working Group 1 meeting # 5", Helsinki, Filand, July 13-16, 1999 (hereinafter referred to as Tsg-Ran).

18. As per claims 17, 18 and 25, Dahlman-Ogawa teaches a forward multiple scrambling code generating apparatus as applied above [see claim 14]. Dahlman-Ogawa is silent on the number of primary scrambling codes, where N is 512 and M is 16. However, TSG-RAN teaches a multiple a code generating apparatus, including generating codes consisting of scrambling codes 1..,512 [see TSG-RAN, options 1 and 2]. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to select scrambling codes where N is 512 and M is 16 as suggested by TSG-RAN and modify Dahlman-Ogawa in order to

generate scrambling codes by selecting scrambling codes from different combination of scrambling code sets.

19. Claims 4-12 are rejected by 35 U.S.C 103(a) as being unpatentable over TSGR1#6(99)915, "TSG-RAN Working Group 1 meeting # 5", Helsinki, Filand, July 13-16, 1999 (hereinafter referred to as Tsg-Ran) in view of Ogawa et al. US Patent 6,738,411 B1 (hereinafter Ogawa).

20. As per claim 4, Tsg-Ran teaches a forward multiple scrambling code generating apparatus, comprising:

a first shift register, that outputs data for the generation of a primary scrambling code (figures 5, shift register 1, and outputs from register 1 to circle plus) ;

a second shift register, that outputs data for the generation of the primary scrambling code and a secondary scrambling code (figure 1, shift register 2, and outputs from register 2 to 1st and 2nd circle plus that output primary and secondary scrambling codes);

a masking function unit, which receives respective outputs from the first shift register, (figure 5, masking function units, and outputs from register 1 and register 2 to the masking function units), and performs a masking function for the received data to output data for the generation of the secondary scrambling code (figure 5, masking function unit), wherein the primary scrambling code is generated by performing a binary addition of the output from the second shift register to an output from the first shift register (figure 5, outputs from register 1 and register 2 combine in the circle plus and output primary scrambling code), and the secondary scrambling code is generated by performing a binary addition of the output from the masking

function unit to the output from the second shift register (figure 1, outputs from register 2 and masking unit combine in the circle plus and output secondary scrambling code).

Tsg-Ran teaches an 18 bit shift registers having data outputs (figure 5, outputs from shift registers 1 and 2). However, Tsg-Ran does not clearly teach registers shifting bits in response to input of a clock. Ogawa teaches a method for simultaneous plural code series generator and for generating primary and secondary scrambling codes [see abstract] further including shifting the nth primary scrambling code by m times to generate a secondary scrambling code [column 7, line 37-column 10 and figure 5]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings of Ogawa within the system of Tsg-Ran in order to increase efficiency of the system.

21. As per claim 5, Tsg-Ran further teaches the apparatus, wherein the first shift register comprises an 18 bit register, in which a value obtained after a binary addition of an output of a 0-th one of the 18 bits to an output of a 7-th one of the 18 bits is fed back to a 17-th one of the 18 bits (figure 5, 0^{th} and 7^{th} bit of register 1 are logically combined in the circle plus and output of circle plus is feed back to the 17^{th} bit).

22. As per claim 6, Tsg-Ran further teaches the apparatus, wherein the second shift register comprises an 18 bit register, in which a value obtained after a binary addition of outputs from a O-th, 5-th, 7-th, and 10-th one of the 18 bits is fed back to a 17-th one of the 18 bits (figure 5, 0^{th}, 5^{th}, 7^{th} and 10th bit of register 2 are logically combined in the circle plus and output of circle plus is feed back to the 17^{th} bit).

23. As per claim 7, Tsg-Ran teaches a code generating apparatus, comprising:

a first shift register, which outputs a first register output (figures 5, shift register 1, and outputs from register 1 to circle plus) ;

a second shift register, which outputs a second register output (figure 5, shift register 2, and output from register 2 to circle plus); and

a masking, function unit, coupled to receive the first and second register outputs, and output a masking output (figure 5, masking function units, and outputs from register 1 and register 2 to the masking function units), wherein the first register output and the second register output are combined to generate a primary scrambling code (figure 5, outputs from register 1 and register 2 combine in the circle plus and output primary scrambling code), and the second register output and the masking output are combined to generate a secondary scrambling code (figure 1, outputs from register 2 and masking unit combine in the circle plus and output secondary scrambling code). Tsg-Ran teaches an 18 bit shift registers having data outputs (figure 5, outputs from shift registers 1 and 2). However, Tsg-Ran does not clearly teach registers shifting bits in response to input of a clock. Ogawa teaches a method for simultaneous plural code series generator and for generating primary and secondary scrambling codes [see abstract] further including shifting the nth primary scrambling code by m times to generate a secondary scrambling code [column 7, line 37-column 10 and figure 5]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings of Ogawa within the system of Tsg-Ran in order to increase efficiency of the system.

24. As per claim 8, Tsg-Ran further teaches the apparatus, wherein the first register output and the second register output are combined using binary addition and output primary scrambling code (figure 5, outputs from register 1 and register 2 combine in the circle plus

(binary addition logical symbol), and output from circle plus), and the second register output and the masking output are combined using binary addition (figure 1, outputs from register 2 and masking unit combine in the circle plus (binary addition logical symbol), and output secondary scrambling code).

25. As per claim 9, Tsg-Ran further teaches the apparatus, wherein the first register output is generated by logically combining selected bits of the first shift register and feeding a result back to a prescribed bit of the first shift register (figure 5, 0^{th} and 7^{th} bit of register 1 are logically combined in the circle plus and output of circle plus is feed back to the 17^{th} bit).

26. As per claim 10, Tsg-Ran further teaches the apparatus, wherein the first shift register comprises an 18 bit register, and wherein the selected bits comprise a 0-th and seventh one of the 18 bits and the prescribed bit is a 17-th one of the 18 bits (figure 5, 0^{th} and 7^{th} bit of register 1 are logically combined in the circle plus and output of circle plus is feed back to the 17^{th} bit).

27. As per claim 11, Tsg-Ran further teaches the apparatus, wherein the second register output is generated by logically combining selected bits of the second shift register and feeding a result back to a prescribed bit of the second shift register (figure 5, 0^{th}, 5^{th}, 7^{th} and 10^{th} bit of register 2 are logically combined in the circle plus and output of circle plus is feed back to the 17^{th} bit).

28. As per claim 12, Tsg-Ran further teaches the apparatus, wherein the second shift register comprises an 18 bit register, and wherein the selected bits comprise a 0-th, 5-th, 7-th, and 10-th one of the 18 bits, and the prescribed bit comprises a 17-th one of the 18 bits (figure

5, 0th, 5th, 7th and 10th bit of register 2 are logically combined in the circle plus and output of circle plus is feed back to the 17th bit).

Allowable Subject Matter

29. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Beemnet W. Dada whose telephone number is (571) 272-3847. The examiner can normally be reached on Monday - Friday (9:00 am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Beemnet Dada

June 7, 2006

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